## AMENDMENTS

**In the Claims:**

The status of each claim is set forth below pursuant to the Revised Format of Amendments. Entry is respectfully requested.

1. (Canceled)

2. (Currently Amended) ~~An FIR~~ A Finite Impulse Response (FIR) filter comprising:

a selection control means for selecting input data, the selection control means including:

a first n-bit shift register (n being a natural number) for progressively shifting the input data through successive stage bits,

n switching means respectively provided for outputs of the n stage bits of the n-bit shift register for controlling the outputs of these n bits, and

a control means for controlling the n switching means, the control means outputting n unique control signals respectively to the n switching means, the control means further being constituted by a second n-bit shift register for shifting a ramp-up/-down signal through successive bit stages under control of a shift clock for the first n-bit shift register; and

a multiplying means for multiplying data selected by the selection control means and a predetermined filter coefficient,

wherein a FIR filter output is derived from the product outputs of the n multiplying circuits means.

3. (Currently Amended) The FIR filter according to claim 2, wherein:

~~the control means is constituted by a second n-bit shift register for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock for the first n-bit shift register; and~~ the n switch means are each an AND gate for receiving the outputs of the corresponding bit stages of the first and second n-bit shift registers as respective inputs.

4. (Currently Amended) The FIR filter according to claim 2, wherein~~:~~

~~the control means is a second n-bit shift register for shifting a ramp-up/-down signal on the basis of the shift clock signal of the first n-bit shift register; and~~ the n switching means are n switches provided for bit stages of the second n-bit shift register for selectively feeding out the filter coefficient data and zero data ~~on the basis of~~ in response to the outputs of the corresponding bit stages.

5. (Currently Amended) The FIR filter according to claim 2, wherein the ~~control means is a second n-bit shift register for shifting a ramp-up/-down signal through the successive bit stages under control of a shift clock signal for the first n-bit shift register, wherein~~ outputs of the bit stages of the first n-bit shift register are reset on the basis of the outputs of the corresponding bit stage of the second n-bit shift register.

6. (Previously Presented) The FIR filter according to claim 2, which further comprises a means for changing a shift clock frequency of the first n-bit shift registers.

7. (Currently Amended) The FIR filter according to claim 2, wherein ~~the control means includes a second n-bit shift register, wherein~~ the shifting operation of the first and second n-bit shift registers are operated under control of shift clock signals at different frequencies.

8. (Currently Amended) The ~~An~~ FIR filter according to claim 3, further comprising an adder circuit for adding together the outputs of the n multiplying circuits, wherein a ramp-up signal is fed to the first n-bit shift register, the ramp-up data being derived from the sum output of the adder circuit.

9. (Currently Amended) The ~~An~~ FIR filter according to claim 3, further comprising an adder circuit for adding together the outputs of the n multiplying circuits, wherein a ramp-down signal is fed to the first n-bit shift register, the ramp-down data being derived from the sum output of the adder circuit.

10. (Currently Amended) ~~An FIR~~ A Finite Impulse Response (FIR) filter comprising:

a first n-bit shift register that receives an input signal and outputs n first-register output signals;

a control circuit that outputs n unique control signals;

an n-bit combining circuit coupled to the first n-bit shift register and coupled to the control circuit, the combining circuit combining the n output signals of the first n-bit shift register with the n unique control signals of the control circuit, the n-bit combining circuit outputting a combining circuit output signal;

n multipliers coupled to the n-bit combining circuit, each of the multipliers multiplying the combining circuit output signals with n filter coefficients, each of the n multipliers outputting a product; and

an adder coupled to the n multipliers, the adder adding the products of the n multipliers.

11. (Previously Presented) The FIR filter according to claim 10, wherein the combining circuit consists of n logic gates.

12. (Previously Presented) The FIR filter according to claim 11, wherein the logic gates are AND gates.

13. (Previously Presented) The FIR filter according to claim 10, wherein an input to the control circuit is a ramp-up/ramp-down signal.

14. (Previously Presented) The FIR filter according to claim 10, wherein the control circuit includes a second n-bit shift register.

15. (Previously Presented) The FIR filter according to claim 14, wherein an input to the control circuit is a ramp-up/ramp-down signal.

16. (Previously Presented) The FIR filter according to claim 10, further comprising:

a second clock signal supplied to the first n-bit shift register; and

a first clock signal supplied to the control circuit;

wherein the second clock signal has a different frequency than the first clock signal.

17. (Currently Amended) ~~An FIR~~ A Finite Impulse Response (FIR) filter comprising:

a first n-bit shift register that receives an input signal and outputs a first-register output signal;

a control circuit that outputs n unique control signals;

n switching circuits, each switching circuit comprising:

a circuit for producing a fixed value;

a circuit for producing a FIR filter coefficient;

a switch coupled to the control circuit, coupled to the fixed value circuit and coupled to the FIR filter coefficient circuit, each switch selecting either the fixed value or the FIR filter coefficient depending upon the control circuit output signal, outputting a switch selection output;

a multiplier coupled to the switch and coupled to the first n-bit shift register, the multiplier multiplying the switch selection output with a selected one of the n first-register output signals to produce a switching circuit output; and

an adder coupled to the n switching circuits, the adder adding the outputs of the n switching circuits.

18. (Previously Presented) The FIR filter according to claim 17, wherein an input to the control circuit is a ramp-up/ramp-down signal.

19. (Previously Presented) The FIR filter according to claim 17, wherein the control circuit includes a second n-bit shift register.

20. (Previously Presented) The FIR filter according to claim 19, wherein an input to the control circuit is a ramp-up/ramp-down signal.

21. (Previously Presented) The FIR filter according to claim 17, further comprising:

a second clock signal supplied to the first n-bit shift register; and

a first clock signal supplied to the control circuit;

wherein the second clock signal has a different frequency than the first clock signal.